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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/724,835	12/02/2003	Takeshi Osada	12732-184001	2791
26171	7590 07/14/2005		EXAM	INER
FISH & RICHARDSON P.C. P.O. BOX 1022 MINNEAPOLIS, MN 55440-1022			TANG, MINH NHUT	
			ART UNIT	PAPER NUMBER
			2829	
			DATE MAILED: 07/14/2003	5

Please find below and/or attached an Office communication concerning this application or proceeding.

SV X

	Application No.	Applicant(s)				
Office Action Comments	10/724,835	OSADA, TAKESHI				
Office Action Summary	Examiner	Art Unit				
	Minh N. Tang	2829				
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply						
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).						
Status						
1) Responsive to communication(s) filed on <u>02 De</u>	ecember 2003.					
2a) ☐ This action is FINAL . 2b) ☒ This	This action is FINAL. 2b)⊠ This action is non-final.					
· · · · · · · · · · · · · · · · · · ·	☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is					
closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.						
Disposition of Claims						
4) Claim(s) 1-8 is/are pending in the application.						
4a) Of the above claim(s) is/are withdraw	n from consideration.					
5) Claim(s) is/are allowed.						
6)⊠ Claim(s) <u>1-8</u> is/are rejected.						
7) Claim(s) is/are objected to.	alastian rasuiramant					
8) Claim(s) are subject to restriction and/or	election requirement.					
Application Papers						
9) The specification is objected to by the Examiner	·.					
10)⊠ The drawing(s) filed on 02 December 2003 is/ar	re: a)∏ accepted or b)⊠ objecte	ed to by the Examiner.				
Applicant may not request that any objection to the o						
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).						
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.						
Priority under 35 U.S.C. § 119						
12)⊠ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a)⊠ All b)□ Some * c)□ None of:						
1.⊠ Certified copies of the priority documents have been received.						
2. Certified copies of the priority documents have been received in Application No						
3. Copies of the certified copies of the priority documents have been received in this National Stage						
application from the International Bureau (PCT Rule 17.2(a)).						
* See the attached detailed Office action for a list of the certified copies not received.						
Attachmant/s)						
Attachment(s) 1) Notice of References Cited (PTO-892) 4) Interview Summary (PTO-413)						
2) Notice of Draftsperson's Patent Drawing Review (PTO-948) Paper No(s)/Mail Date						
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 12/02/03.	5) Notice of Informal P	atent Application (PTO-152)				
S. Patent and Trademark Office						

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

- 2. The information disclosure statement (IDS) submitted on December 02, 2003 is considered by the examiner.
- 3. The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A(1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

Drawings

4. Figure 7A should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

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5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: reference numbers "113", "114", and "115" (see Applicant's specification page 6, lines 28-29). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

- The disclosure is objected to because of the following informalities:
 a/ on page 1, line 18, a period should be placed before "The image".
 b/ on page 3, line 4, a period should be placed at the end of the sentence.

 Appropriate correction is required.
- 7. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

8. Claims 6 and 7 are objected to because of the following informalities: in claims 6 and 7, all in line 1, "A method for testing an image display device" should be -- An image display device --.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
- 10. Claims 1-8 are rejected under 35 U.S.C. 102(a) as being anticipated by the admitted Prior Art Figs. 3-4 and 7A-7B (hereinafter the admitted Prior Art).

As to claim 1, the admitted Prior Art discloses an image display device comprising: a pixel portion (704) comprising a display region (704a) and a testing region (704b), wherein the display region (704a) and the testing region (704b) comprises a first pixel circuit (705a) and a second pixel circuit (705b), respectively; each of the first and second pixel circuits (705a, 705b) comprising: a data signal line (711); a scanning line (712); a driver transistor (714); and a switching transistor (713) provided between the data signal line (711) and a gate electrode of the driver transistor (714), wherein a gate electrode of the switching transistor (713) is electrically connected to the scanning line (712), wherein the driver transistor (714) of the first pixel circuit (705a) is provided between a current supply line (717) and a light emitting element (716), and wherein the

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driver transistor (714) of the second pixel circuit (705b) is provided between the current supply line (717) and a testing terminal (315a, 315b, Fig. 3).

As to claims 2 and 4, the admitted Prior Art discloses, the testing region (704b) is provided in a dummy pixel region which is provided in an outer edge region of the pixel portion (704).

As to claim 3, the admitted Prior Art discloses an image display device comprising: a pixel portion (704) comprising a display region (704a) and a testing region (704b), wherein the display region (704a) and the testing region (704b) comprises a first pixel circuit (705a) and a second pixel circuit (705b), respectively; the first pixel circuit (705a) comprising: a data signal line (711); a scanning line (712); a driver transistor (714) provided between a current supply line (717) and a light emitting element (716); and a switching transistor (713) provided between the data signal line (711) and a gate electrode of the driver transistor (714); and the second pixel circuit (705b) comprising: the data signal line (711); the scanning line (712); and the switching transistor (713) provided between the data signal line (711) and a testing output terminal (315a, 315b, Fig. 3), wherein a gate electrode of the switching transistor (713) of the first pixel circuit (705a) is electrically connected to the scanning line (712).

As to claim 5, the admitted Prior Art disclose an image display device comprising: a pixel portion (704) comprising a display region (704a) and a testing region (704b), wherein the display region (704a) and the testing region (704b) comprises a first pixel circuit (705a) and a second pixel circuit (705b), respectively; each of the first and second pixel circuits (705a, 705b) comprising: a data signal line (711); a scanning line

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(712); a driver transistor (714); and a switching transistor (713) provided between the data signal line (711) and a gate electrode of the driver transistor (714), wherein a gate electrode of the switching transistor (713) is electrically connected to the scanning line (712), wherein the driver transistor (714) of the first pixel circuit (705a) is provided between a current supply line (717) and a light emitting element (716), wherein the driver transistor (714) of the second pixel circuit (705b) is provided between the current supply line (717) and a testing terminal (315a, 315b, Fig. 3), and wherein the scanning line (712) is placed in a selected state to provide a conduction to the switching transistor (713) in the second pixel circuit (705b) and a drain current of the driver transistor (714) is outputted to the testing output terminal (315a, 315b) according to the signal outputted to the data signal line (711).

As to claim 6, the admitted Prior Art Fig. 3 discloses, a signal (video signal VData) outputted to the data signal line (711) is a video signal.

As to claim 7, the admitted Prior Art Fig. 3, a signal outputted to the data signal line (711) is a testing pulse.

As to claim 8, the admitted Prior Art discloses an image display device comprising: a pixel portion (704) comprising a display region (704a) and a testing region (704b), wherein the display region (704a) and the testing region (704b) comprises a first pixel circuit (705a) and a second pixel circuit (705b), respectively; the first pixel circuit (705a) comprising: a data signal line (711); a scanning line (712); a driver transistor (714) provided between a current supply line (717) and a light emitting element (716); and a switching transistor (713) provided between the data signal line (711) and a gate

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electrode of the driver transistor (714); the second pixel circuit (705b) comprising: the data signal line (711); the scanning line (712); and the switching transistor (713) provided between the data signal line (711) and a testing output terminal (315a, 315b, Fig. 3), wherein a gate electrode of the switching transistor (713) of the first pixel circuit (705a) is electrically connected to the scanning line (712), and wherein the scanning line (712) is placed in a selected state to provide a conduction to the switching transistor (713) in the second pixel circuit (705b) and output the signal which is outputted to the data signal line (711) to the testing output terminal (315a, 315b).

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Inukai	US 2001/0038367 A1	Light Emitting Device.
Koyama	6,762,735	Electro Luminescence Display Device
		And Method Of Testing The Same.
Koyama	6,809,482	Light Emitting Device And Method Of
		Driving The Same.
Tanada	6,909,409	Electronic Device And Method Of
		Driving The Same.

Communication

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh N. Tang whose telephone number is (571) 272-1971. The examiner can normally be reached on M-F (7:00-3:30).

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor R. Ramirez can be reached on (571) 272-2034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MINH NHUTTANG PRIMARY EXAMINER

7/07/05